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IMPLEMENTATION OF EFFICIENT TRUNCATED BOOTH MULTIPLIERS

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Abstract

The project focuses on optimizing multiplication in digital system by employing truncated booth encoding for enhanced efficiency. Through a systematic approach, it defines design specifications, implements using cadence tool, and rigorously tests at various stages. Results demonstrate significant improvements in hardware efficiency and performance compared to conventional methods, particularly beneficial for applications like digital signal processing and communications. This research contributes to advancing digital design methodologies, paving the way for more efficient multiplication techniques in future electronic systems.

Keywords — *Truncated booth multipliers, Area and power efficient , Xilinx, partial product, FPGA design.*

I. INTRODUCTION

In DSP,efficient multiplication is critical, with multipliers often determining system speed. While precision is vital, some applications tolerate errors, allowing for approximate arithmetic units. These approximate multipliers typically address partial product accumulation, aiming to reduce delay and hardware overhead, recent advances include error compensation strategies and innovation methodologies like modifying karnaugh maps and utilizing dadda trees to enhance efficiency. This paper explores the evolution of approximate multipliers, focusing on booth multipliers, and approaches to improve efficiency and accuracy. Simulation results demonstrate superior performance, particularly in speed, power efficiency and circuit area. Practical applications in low-pass finite impulse response (FIR) filters further underscore their effectiveness.

II. LITERATURE SURVEY

[1] The primary objective of this study is to develop truncated booth multipliers that are both area and power efficient. The focus is on reducing the hardware footprint while maintain high performance. Xilinx software is utilized to implement these multipliers, leveraging its synthesis and optimization capabilities. [2] Another aim is to optimize the power consumption of truncated booth multipliers without sacrificing performance. This involves careful design considerations and utilization of Xilinx tools for power analysis and optimization. [3] The goal of this approach is to ensure that area-efficient truncated booth multipliers can be seamlessly integrated into FPGA designs. Xilinx software provides a platform for efficient synthesis and implementation, enabling the integration of these multipliers into larger digital systems. [4] This study explores techniques for achieving both area and power efficiency in truncated booth multipliers using Xilinx's Vivado design suite. By leveraging advanced synthesis and optimization features, the researches aim to minimize resource utilization and power extent while maximizing performance. [5] The main objective of this paper is to provide a comprehensive analysis of area and power-efficient truncated booth multipliers implemented using Xilinx software. Through synthesis, optimization, and performance evaluation, the study aims to demonstrate the effectiveness of these multipliers in FPGA-based designs.

III.OBJECTIVES

1. To design a Quarternary booth multipliers for Low-Power and High-Performance operation.
2. To perform a signed multiplication by encoding and thereby reducing the number of partial products.
3. To reduce the system process time and increase the speed of process.

IV. METHODOLOGY

The methodology comprises several key components. It begins with the generation of partial products

using an encoder, followed by the utilization of Radix-4 Booth multiplier to efficiently handle multiplication operations. The accumulated partial products are then processed to derive the final result, with data processing facilitated by D-register architecture for sequential operation. An approximate partial product matrix is employed to balance computational speed and accuracy. An error correction operation block corrects any inaccuracies introduced during computation. Subsequently,the design undergoes final simulation and synthesis analysis for performance evaluation. Efficiency is further enhanced through the integration of truncated techniques in Booth multipliers,alongside measures to optimize power consumption,manage clock signals,and implement parallel multiplier architecture. Performance metrics are evaluated to validate the effectiveness of the methodology.

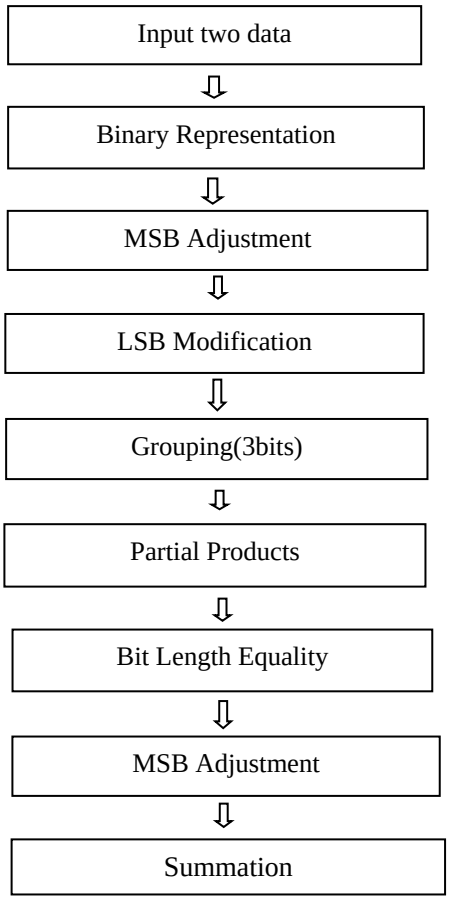

Fig. 1 Flow Chart

ALGORITHM

1. **Input:** Choose two even-bit signed or unsigned numbers,A and B.
2. **Binary Representation:** Write down the binary equivalents of A and B.
3. **MSB Adjustment:** If needed,add an extra bit to the leftmost leading bit of the larger number.
4. **LSB Modification:** Select one number,let`s say A,and add an extra 0 to the LSB.
5. **Grouping:** Group the modified A and B in bits of 3,shifting one bit to the left in each group.
6. **Partial Products:** Use a truth table to generate unique multiplication result for each bit
7. **Bit Length Equality:** Ensure equal bit lengths for unequal bits by adding leading zeros or ones.
8. **MSB Adjustment:** Add any necessary bits leading to the leftmost side based on MSB of the original numbers.
9. **Summation:** Sum up the modified partial products in order to obtain final output.

In summary, our methodology for designing truncated Booth multipliers combines both a structured flowchart and algorithmic techniques. The flowchart outlines sequential operations involved in the multiplier`s function, ensuring a methodical approach from start to finish.Meanwhile,the algorithmic techniques, such as radix-4 Booth encoding and D-register architecture,provide specific optimizations to improve efficiency and performance.Together, these methodologies contribute to creation extent power-efficient truncated Booth multipliers,demonstrating their effectiveness across different digital design scenarios.

V.RESULTS

1. **Multiplication Output:** The findings of multiplication operation, typically expressed in numerical form.
2. **Schematic Diagram:** A visual of the depiction of the system ,detailing its components and connections.
3. **Space and Energy Report:** An analysis of the physical area occupied by the design and the power consumption it entails,crucial for optimizing efficiency and performance.

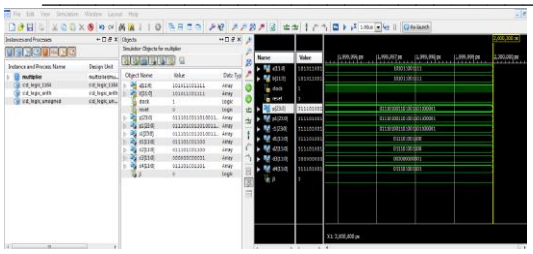

Fig.2 Multiplication Output

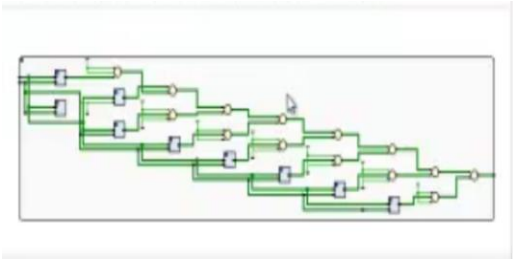

Fig.3 Schematic Diagram

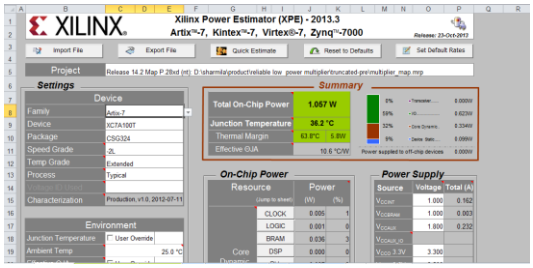

Fig.4 Area and Power Report

VI. CONCLUSION

Truncated Booth multipliers enhance area and power efficiency. Leveraging Xilinx software,we optimized them to reduce hardware footprint while maintains high performance. Seamless integration into FPGA designs showcased their adaptability and effectiveness in various applications. Area and Power efficient multipliers.

A. Advantages

1. Enhanced area efficiency
2. Improved power efficiency
3. High performance
4. Seamless integration
5. Versatile applications

B. Limitations

1. Resource constraints
2. Timing constraints
3. Complexity
4. Power consumption
5. Design tools and optimization
6. Verification and debugging

C. Future Scope

In further days Xilinx software promises efficient Booth multipliers. Research of machine learning and synthesis tools streamline design.Power management and custom instructions optimize tasks.System-level optimization crucial for efficiency. Continued FPGA advancements drive efficiency grains.

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