International Journal of Trendy research in Engineering and Technology(IJTRET)
Volume 2 Issue 2(2) April 2018

DESIGN OF POWER EFFICIENT 18-TRANSISTOR TRUE SINGLE-PHASE CLOCKING FLIP-FLOP

Arul Bharathi R[#1], Kalki B[#2], Parkavi R[#3], Sathyaraj P[#4]
[#]*UG Students , Department of ECE, Arasu Engineering College, Kumbakonam, Tamilnadu,India*[#123]
[#]*Assistant professor, Department of ECE, Arasu Engineering College, Kumbakonam, Tamilnadu*[#4]
kalkibalu1207@gmail.com[#1] vlsisathya@gmail.com[#4]

ABSTRACT: *In the existing flip flop design 19 transistors were used to design. It increases the power consumption delay and time performance. So to reduce the above mentioned problems, an ultralow low power true single phase clocking flip flop design achieved using only 18 transistors is proposed. The transistor count is reduced by using logic structure reduction scheme. In this design master slave logic structure is used and hybrid logic design which comprises of both static CMOS and complementary pass transistor logic. A virtual VDD design technique also employed which facilitates a faster state transition in the slave latch is devised to enhance the time performance. The circuit is implemented using TSMC 0.18µm CMOS technology post layout simulation results indicated that the proposed design excelled in various performance indices such as PDP, clock to Q delay, average power consumption and leakage power consumption. Compared with transmission gate based FF design, the PDP improvement was up to 63%.*

Key words: Complementary pass transistor logic, virtual VDD technique, master slave flip-flop, low power, true single-phase clocking (TSPC).

I. INTRODUCTION

Flip-Flops are storage elements used in digital system design and employ several FF-rich modules such as register files, shift registers and FIFO.The Flip-Flop can store one bit of data. The Flip-Flops uses both static and dynamic logic.It consists of various types, in this paper master slave flip flop is employed to achieve low power FF design.The Flip-Flops are mainly used as a memory storing elements in mobile phones, digital camera and tablet PC.

The flip-Flop family has the capability of easily incorporating logic functions with a small delay penalty.The development of various kinds of wearable information equipment or healthcare associated equipment has newly prospered in recent years. In those kinds of battery working equipment, reduction power is a very important issue, and demand for power reduction in VLSI is increasing. For that various kinds of circuit techniques have already proposed.

The power consumption of the FFs employed in a typical digital system design, along with that clock distribution networks, constitutes as high as 20%-40% of the total system power. In storage elements more than half of the power is dissipated in random logic, of which half of the power is dissipated by flip-flops (FF). FF designs are thus crucial to the power consumption performance of the system design and also have impact on the chip area. Specific application demands such as high speed, low power, and low voltage.

The numerous FF designs have been developed, recent design emphases have switched gradually from ultrahigh-speed toggling to extremely low-power operations.Reducing this redundant switching activity has a profound effect in reducing the power dissipation. Reducing these activities can efficiently result in reducing the overall power consumption. To achieve the low power design it is important to reduce the clock system power.The clock system power is reduced by clock voltage swings.

A. CELL OPERATION

The operation of the Master-Slave flip flop is that clock pulse is ‘0’, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode. Both the voltages VD1 and VD2 are pulled up to power-supply level and the data from D are stored in the master latch. When the clock pulse is ‘1’, the PMOS connected to CP turns off, the NMOS connected to the CP turns on, and the slave latch becomes the data output mode. Then the data stored in the master latch is transferred to the slave latch and then outputted to Q. In this operation, all nodes are fully static and full-swing. The master and slave latch become active alternatively so there is small time degradation on cell performance.

II. LITERATURE SURVEY

In order to reduce the power of the FF, the transistor count is reduced without introducing any dynamic or pre-charge circuit. Most of the power is dissipated in the operation of clock-related transistors, and reduction of transisitor count reduces the load capacitance in internal nodes.In the conventional FF design 12 clock related transistors are used. Because the conventional FF design use transmission gate for both PMOS and NMOS.In this FF design the transmission gate is replaced by combinational type circuit. The count is reduced based on the logical equivalence which has the same input signal combination, including clock signal as the input signal.In the topologically compressed FF (TCFF) obtained through topologically compressed scheme. In this design the master latch is implemented using two AND-OR-Invert (AOI) gates. When the clock is low the master latch is transparent. the input pass through the AOI gates and the output is invert. When the clock is high the slave latch becomes active the data is transferred from the master to the slave and then the output is passed through the two AOI gates and invert. Only one phase of clock signal is used in this design. Figure 1 shows the topologically controlled 21 transistors FF design.

The TCFF design based on use the single clock pulse, reduce the number the transistor driven clock, and reduce the total transistor count. It shows the significant improvement in the power consumption, timing performance. The operating voltage for TCFF is 0.6V/250MHZ.The design suffers longer set up time because of a weakened pull-up network connected directly to VDD.Only three transistors (two PMOS and one NMOS) are driven by the clock signal. The simulation results figure 4 show the output.

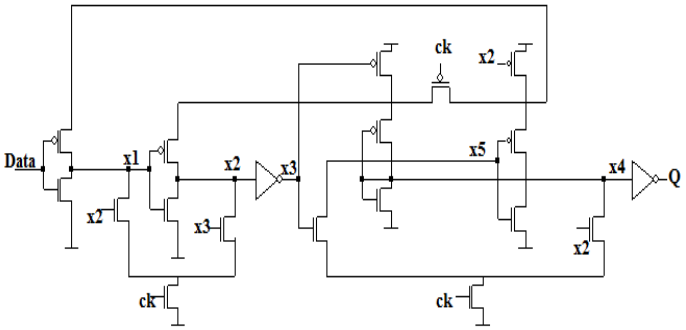

Figure 1. Conventional Flip-Flop

III. EXISTING SYSTEM

In figure 1 the discharging path is connected through the slave latch and controlled by the clock signal. In this paper that discharge path is split into two paths each comprising of two NMOS transistors in series and implementing logic x2.CK.0 and x3.CK.0.The discharging path in the TCFF design can be split into two separate paths, each comprising one pas transistor. Hence, the transistor count is reduced from 21 to 19.The benefit of this logic structure reduction is it simplifies the circuit for power saving.

Data latching process, for the case latching data=1, the master latch is transparent to admit the new data and the slave latch hold its current value. For latching the data=0, the master latch in its hold state and the slave latch changes its value. When the clock is low nodes e and f connected to VDD.When clock=1 the node disconnected from VDD.The operating voltage for LCFF (logic structure reduction FF) is 1V/500MHZ.The design is fully static and full-swing. Figure 2 shows the LCFF design .The simulation result figure 5 shows the output of LCFF.

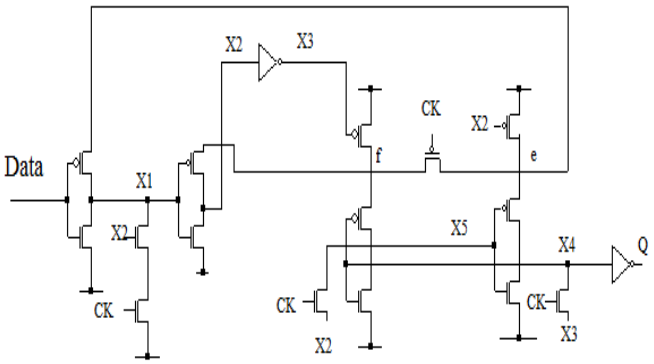

Figure 2: Existing Flip-Flop Design LCFF

IV. PROPOSED SYSTEM

In the proposed system design the transistor count is further reduced from 19 to 18. This reduction simplifies the circuit and the power consumption also reduced. Figure 3 shows the structure of 18 transistor FF design. In this design the transistor in the master latch is combined with the clock signal and thus the transistor count is reduced by one. The

operation involves that when data=0 and clock is low the master latch becomes transparent and stores the data input. When data=1 and clock is high the master is in hold state and the slave latch changes its value that is the data stored in the master is transferred to slave and it is outputted to Q.The operating voltage 0.9V/550MHZ.The clock controlled NMOS transistor is also connected with the x2 discharging node. Hence, the power gets reduced and the delay also compromised. The set up time , hold time are in seconds.

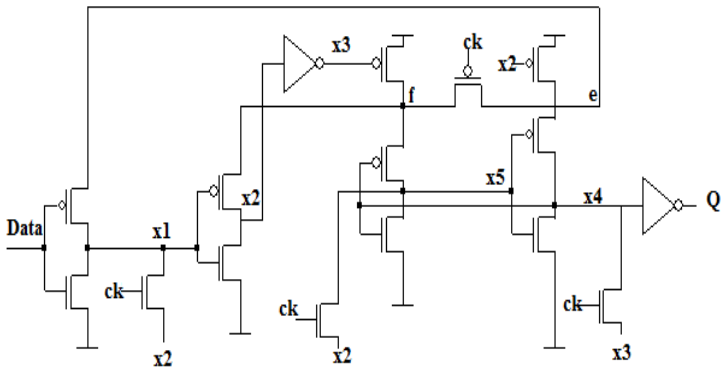

Figure 3: Proposed Flip-Flop design

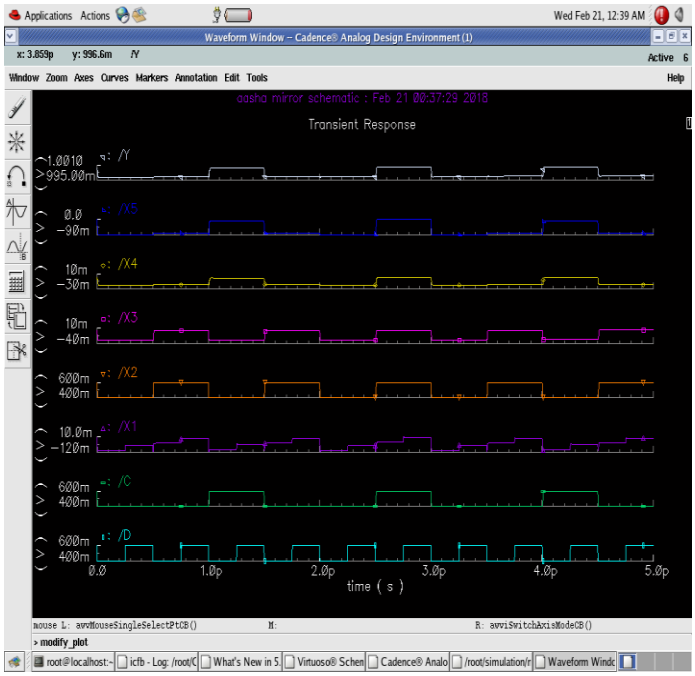

Figure 5: Simulation result of Existing LCFF flip-flop

V. SIMULATION RESULTS

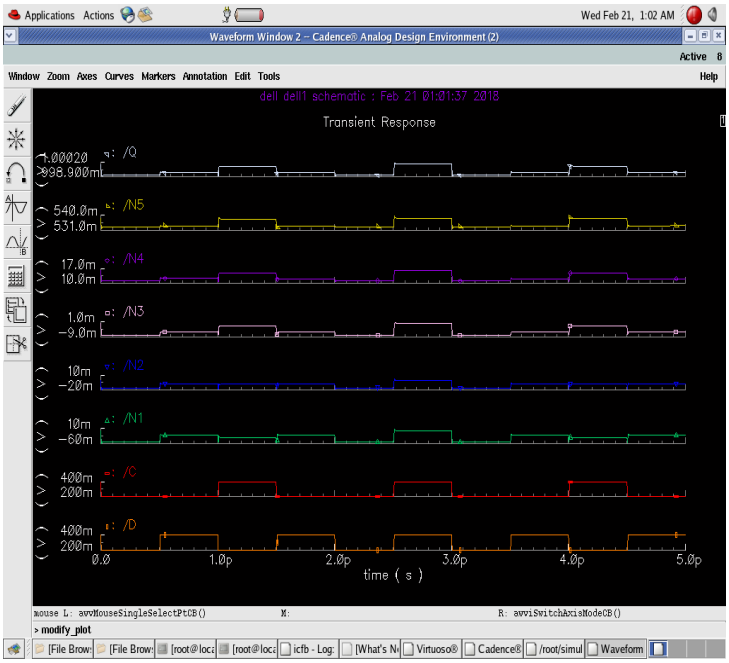

Figure 4 : Simulation result of conventional flip-flop

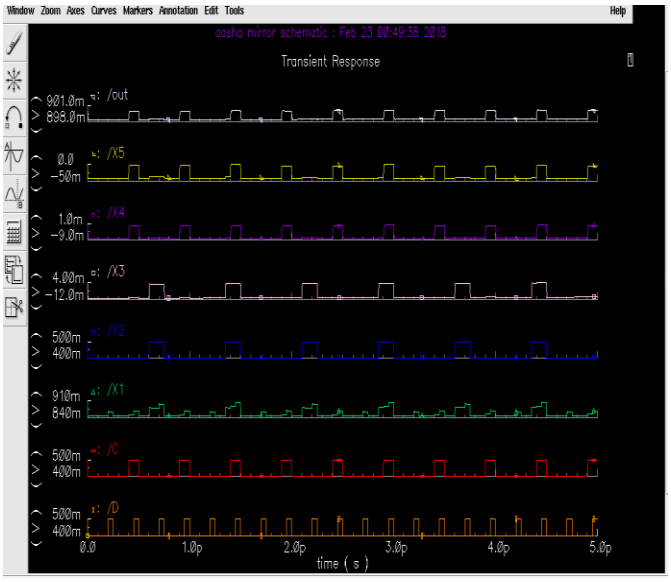

Figure 6: Simulation result of proposed FF design

VI. CONCLUSION

In this paper, FF design is achieved by logic structure reduction employing static CMOS and complementary pass transistor logic. This design providing additional discharge path between the master salve latches, to enhance the speed and power also reduces circuit complexity for better timing performance. Simulations were conducted and various parameter indices such as power consumption, set up time and delay were evaluated.The proposed design consistently outperformed other designs under different voltage and switching activity settings. Thus proves the efficiency of the proposed system design.

REFERENCE

[1] Jin-Fa Lin,Ming-Hwa sheu," Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes"IEEE transient,volume.30,no 8,Jan 2017.

[2] OJ.Furuta, J.Yamaguchi, K.Kobayashi, "Aradiation-hardenednonredundant flip-flop, stacked leveling critical charge flip-flop in a 65 nm thin BOX FD-SOI process,"IEEE transient. Nuclear science., volume. 63, no. 4,pp. , Aug. 2016.

[3] A. Makiharaetal., "Hardness-by-design approach for *0.15* μm fullydepleted CMOS/SOI digital logic devices with enhanced SEU/SET immunity," IEEE transient. Nuclear science, volume 52, no. 6, pp. 2524–2530,Dec. 2005.

[4] R. C. Baumann, "Radiation-induced soft error in advanced semiconductor technologies," IEEE transient Device master. Rel., volume. 5, no. 3, pp. 305–316, Sep. 2005.

[5] N. Kawai, "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," IEEE J. Solid-state, circuit's volume. 49, number 11,pp. 2526-2533, Nov. 2014.

[6] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low-power conditional discharge flip-flop''IEEE Transaction Very Large Integration (VLSI) System volume.12, no.5, pp.477-484, May 2004.

[7] F. Klass et al., "A new family of semidynamic and dynamic flip-flops with embedded logic for high-performance processors," IEEE J. Solid-state Circuits, volume 34, no. 5, pp. 712–716, May 1999.

[8] V. Stojanovic and V. G. Oklobdzija, "Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, volume 34, no. 4, pp. 536–548, Apr. 1999.

[9] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.T. Leung, "Improved sense-amplifier -based flip-flop: Design and measurements," IEEE J. Solid-State Circuits, volume35, no. 6, pp. 876–884, Jun. 2000.

[10] M. Matsui, "A 200 MHz 13 mm2/2-D DCT macro cell using sense amplifying pipeline flip-flop scheme," IEEE J. Solid-State Circuits, volume 29, no. 12, 1482–1490, Dec. 1994.